Ka-band High Efficiency 1 Watt Power Amplifier

G.S. Dow, K. Tan, N. Ton, J. Abell, M. Siddiqui
B. Gorospe, D. Streit, P. Liu, M. Sholley

TRW Electronic Technology Division
One Space Park
Redondo Beach, CA 90278

ABSTRACT

This paper describes the design and performance of a miniaturized 35 GHz power amplifier. The two-stage amplifier has achieved an output power of 1 watt with an associated gain of 10 dB and a power-added efficiency of 25.1%. The design is based on TRW 0.25 μm T- gate Pseudomorphic InGaAs HEMT device technology. The amplifier is designed using a 1 mm device driving a 2 mm device. The complete amplifier mounted on a carrier measures 0.26" x 0.16" x 0.02". The amplifier results reported here represent the best power gain and efficiency performances achieved from a single amplifier at 35 GHz.

I. INTRODUCTION

Future millimeter-wave phased array antenna or terminal guided missile systems require power amplifiers with output power ranges from several watts to tens of watts. Additional requirements for these amplifiers include low dc power consumption and small size. To achieve these goals, effective combining of high performance power amplifier units that have good output power capability (~1 watt) and power-added efficiency (> 20%) performances are required. Millimeter-wave power combining techniques have been discussed previously and the design approach is well understood [1,2]; however, few reported results of power amplifiers with more than 1 watt of output power performance . In the cases where these results were reported, they were attained by combining several low level power amplifier and suffered low gain and low efficiency performances [3,4].

In this paper, we present the results of a high performance 35 GHz 2-stage power amplifier that has demonstrated an output power of 1 watt , an associated gain of 10 dB and a power added efficiency of 25.1 %. It uses a 1 mm InGaAs HEMT device driving a 2 mm InGaAs HEMT device. The complete amplifier mounted on a carrier measures only 0.26"x0.16"x0.02".

II. PM InGaAs POWER HEMT DEVICE

The device used in this work is a pseudomorphic InGaAs 0.25 μm T-gate device. The device profile used is a double heterojunction power HEMT grown using molecular beam epitaxy. Silicon planar doping was employed on both heterojunctions to provide carriers to the InGaAs channel. Figure 1 shows the device cross-section. Hall mobility measurements measured on calibration wafers indicate a 300 °K 2-dimensional electron sheet charge density of 2.84×10^{12} cm^{-2} with a mobility of 4060 cm^2/V-s. The device layout uses airbridges to connect the source pads external to ground vias. This device layout allows for a more compact device design. The completed devices are thinned to 30 μm and employ 10 μm plated back metal to provide low thermal resistance. Figure 2 shows the SEM photo of a 500 μm device.

The completed devices typically have full channel currents of greater than 600 mA/mm at a drain bias of 2 V and a gate voltage of +0.8 V. The average transconductance of this wafer was 506 mS/mm with a average cut-off frequency ft and fmax of 52.7 and 110 GHz, respectively. The undoped AlGaAs used allows for high gate breakdowns, for this wafer the gate-drain breakdown voltage was greater than 10 V (defined at 100 μA/mm). The excellent device breakdown, together with the high current density and high device gain, results in power added efficiency of 40% measured on a 500 μm device. The output power at this maximum efficiency condition was 307 mW (615 mW/mm) with 6.8 dB gain.

III. POWER AMPLIFIER DESIGN

The two-stage amplifier design uses a 1mm device driving a 2 mm device. Each device is constructed using a 500 μm unit cell with gate finger width of 50 μm. The circuit topology is selected to perform both in-phase divide/ combine and device impedance matching functions simultaneously. For simplicity of

CH3141-9/92/0000-0579$01.00 © 1992 IEEE

implementation, only transmission line circuit elements were used. Figure 3 shows the circuit schematic of the two-stage amplifier. The input matching network of the 1 mm device is implemented with both a 10 mils thick Al_2O_3 and a 2 mils thick GaAs substrates. The later is used to realize the low impedance transmission line required for the close-in cell level divider/matching network. This implementation allows the close-in network to match to the device impedance while maintaining physical compatability. The remaining input matching network, which includes the bypass decoupling network, is realized with 10 mils Al_2O_3 substrate . To terminate the odd mode interaction between the cells, NiCr isolation resistor is placed between the two close-in transmission lines. The interstage matching network which matches the output impedance of the 1 mm device to the input of the 2 mm device is also realized with a 10 mils thick Al_2O_3 and a 2 mils thick GaAs substrates. The close-in divider/matching section for the 2 mm device, which is realized with 2 mils thick GaAs substrate, has a binary-tree topology to divide the input power equally among the four 500 μm cells. The remaining interstage matching network, which includes the output matching network for the 1 mm device, a dc block realized with coupled transmission line and two bypass decoupling networks, is realized with 10 mils Al_2O_3 substrate . Finally, the output matching network, which combines the output of two 1 mm cells while providing the necessary large signal match, is also realized also with 10 mils Al_2O_3 substrate. Figure 4 shows a circuit layout of the complete amplifier.

The complete amplifier, including the external bias and decoupling networks, were mounted on a gold plated Cu-carrier. The complete amplifier carrier measures only 0.26"x0.16"x0.02". The compactness of this unit makes it particularly suited for power combining to achieve higher level of output power.

III. TEST RESULTS

For RF evaluation, the amplifier is mounted on a specially designed test fixture with waveguide interfaces, as shown in Figure 5. The input and output interfaces to the waveguide are E-plane probe transitions. Measured insertion of two E-plane probe transitions with a back-to-back connection is 0.6 dB at 35 GHz.

The amplifier is biased at a drain voltage of +5 V supply. Both stages are biased at about 75% Idss. Figure 6 shows the Pin vs Pout and power added efficiency performances of the amplifier at 34.5 GHz . With Pin=20 dBm, the amplifier achieves an output power of 30 dBm. The DC currents for the two stages are 220 mA and 498 mA, respectively. This corresponds to a power-added efficiency of 25.1 %. The linear gain for the amplifier is 14.5 dB. These results represent the best reported power gain and efficiency performances achieved from a single amplifier for these frequency of operation. Figure 7 shows the frequency responses of the amplifier from 33.5 GHz to 35.5 GHz with a varied Pin from 10 to 17 dBm. The highest gain occurs at 34.5 GHz. With a Pin=17 dBm, an output power of 29.8 dBm is achieved at this frequency.

VII. SUMMARY

We have reported the design and test results of a Ka-band two-stage power amplifier using 0.25 μm Pseudomorphic InGaAs HEMT device technology. The amplifier uses a 1 mm device driving a 2 mm device and has achieved an output power of 1 watt, an associated gain of 10 dB and a power added efficiency of 25.1%. The close-in divider/matching network is realized with 2 mils thick GaAs substrate. This approach allows simultaneous electrical and physical match to a large device. The small size of this circuit makes it particularly suited for power combining to achieve higher level of output power. The same circuit design also can be implemented as a monolithic circuit.

ACKNOWLEDGEMENTS

The authors would like to express their gratitude to the people who has contributed in this work : M. Aust, D. Pham, S. Chan, J. Coakley, T. S. Lin and T. Trinh. We also thank Dr. B. Allen, Dr. J. Raue and Mr. R. Dixit for their continuous support and guidance.

REFERENCES

[1] D.I. Stones, P.D. Chow, "Q- and V-Band Planar Combiners," *IEEE MTT-S Int. Microwave Symp. Dig*, June 1991, pp 1049-1052.

[2] G.W. Swift, D.I. Stones, "A comprehensive Design Technique For The Radial Wave Power Combiner," in *IEEE MTT-S Int. Microwave Symp. Dig.* June 1988, pp 279-281.

[3] S. Arai, T. Yoshida, K. Kai, S. Takatsuka, Y. Ada and S. Yanagawa, "Ka-Band 2-Watt Power GaAs MMIC," in *IEEE MTT-S Int. Microwave Symp. Dig*, June 1989, pp 1105-1108.

[4] C. Creamer, P. Chye, B. Sinclair, "43.5 to 45.5 GHz Active Times-4 Frequency Multiplier With 1.4 W Output Power," in *IEEE MTT-S Int. Microwave Symp. Dig*, June 1991, pp 939-942.

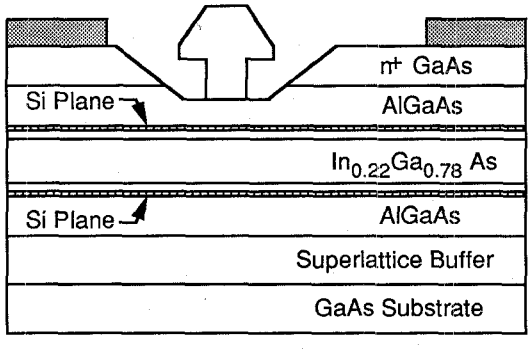

Figure 1 Power HEMT device cross-section

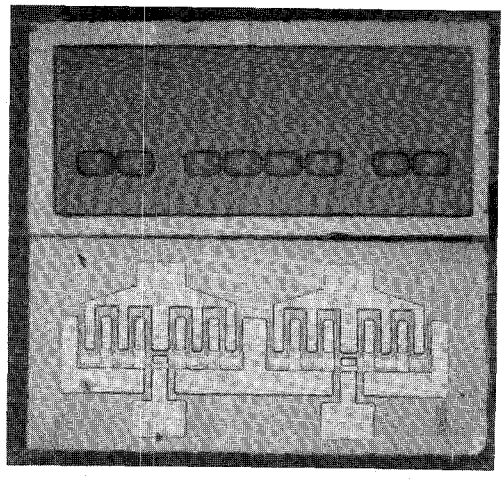

Figure 2 SEM photo of a 1 mm device consists of two 500 μm cells

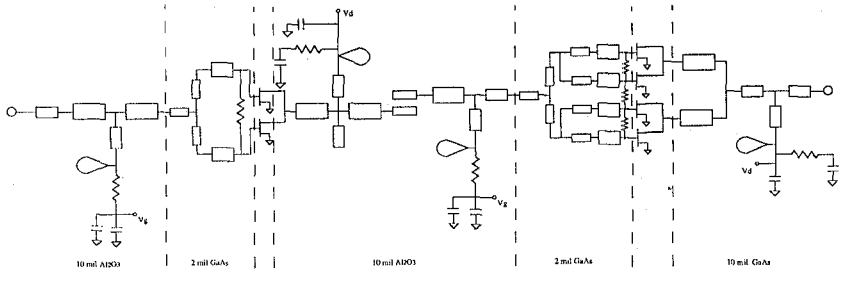

Figure 3 Circuit schematic of the 2-Stage power amplifier

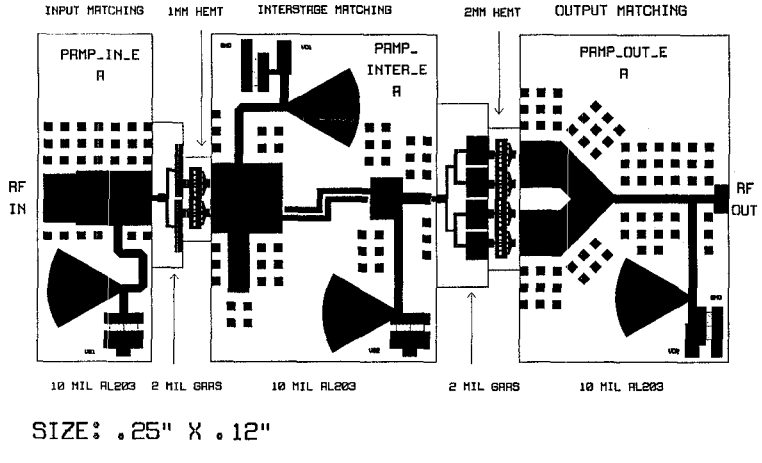

Figure 4 Circuit layout of the 2-stage amplifier

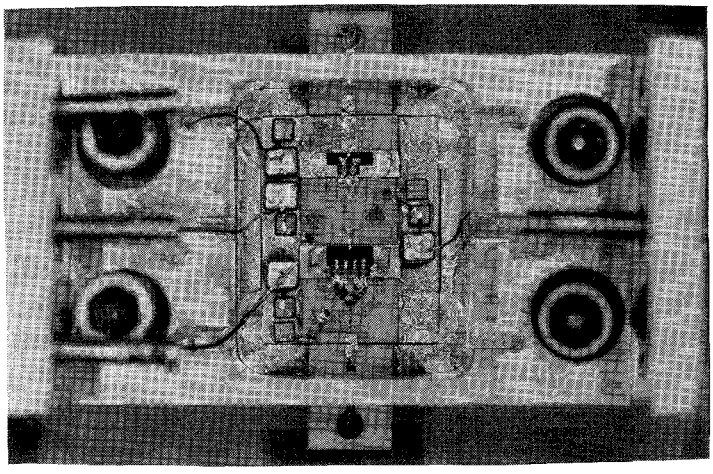

Figure 5 Photo of the amplifier mounted inside a test fixture with E-probe transitions

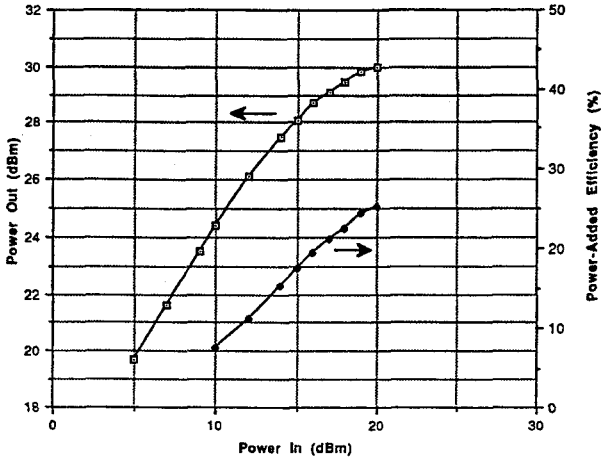

Figure 6 Amplifier Pin vs Pout responses at 34.5 GHz

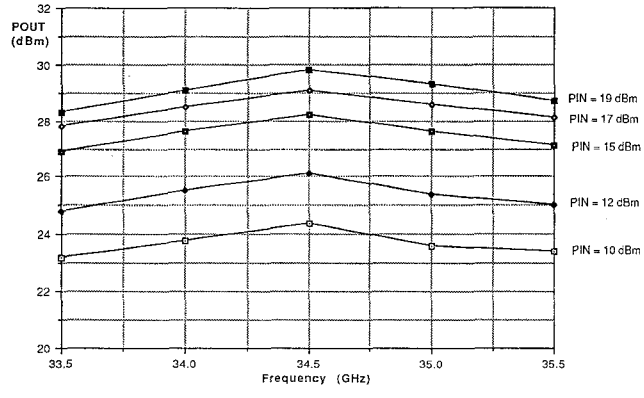

Figure 7 Amplifier frequency responses as a function of Pin